Area: Crystalline and Thin Film Silicon PV

PECVD LAYERS FOR HIGH AND LOW TEMPERATURE IMPROVED INDUSTRIAL SOLAR CELL PROCESSES

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A determining upgrade of production lines towards higher solar cell efficiencies relies on contact area reduction *e.g* in PERC architecture. The implementation of PECVD layers in solar cell process flow enables highly performing alternative approaches for standard line upgrade; either in an evolutionary approach with temperature stable layers implemented for instance as full area rear electrode or in a more disruptive approach with silicon heterojunction (SHJ) technology. The potential of SHJ technology to reach high conversion efficiencies is well known, emphasized recently by outstanding results by Kaneka. Semi-insulating polycrystalline (SIPOS) like approaches have also demonstrated their performance advantages. In this work, high and low temperature cell architectures based on PECVD and associated developments to enable high device performance, maintaining a simple process flow, are presented.

Mastering PECVD deposition parameters enables the deposition of uniform, reproducible passivating intrinsic and doped a-Si:H layers enabling state-of-the-art passivation levels, with lifetime values on par with the actual theoretical limit for Auger recombination over a broad range of injection levels (Fig. 1), leading to iVoc ~735mV on n-type, 150um thick, Cz wafers. Here, PECVD regimes are developed in a large-area (35 x 45 cm^2) multi-chamber reactor. As shown in Fig. 2, integrating these layers into a low temperature industrial SHJ architecture enable to achieve above 23% (Fig. 2). In addition to SHJ solar cells, PECVD expertise turns to be useful as well for alternative high-efficiency and temperature stable cell structures. Various types of such layers are being developed jointly with EPFL. A firable hole-selective rear contact is one example currently being fine-tuned and integrated for industrial use. 150um thick, 2 Ohm.cm p-type 6" Cz wafers symmetrically passivated with such layer stacks enable already iVoc > 715mV and J0e <20fA/cm^2. Efficient carrier extraction is demonstrated resulting in FF values exceeding 79% when implemented in a cell featuring an i/na-Si:H front side [A. Ingenito, this conference]. Integrating this layer as fully passivated rear side electrode, combined with optimized front side $POCl_3$ emitter (~65fA/cm^2) is anticipated to enable device V_{oc} values >680mV accounting for a 5% metal fraction on the front side.

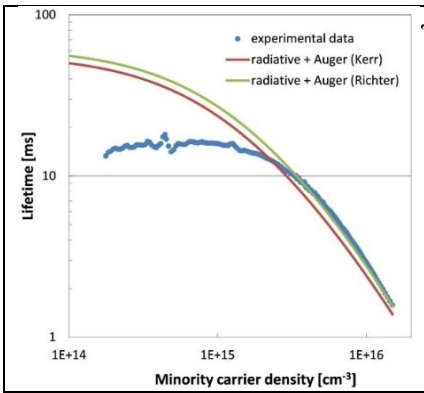

Fig. 1. Minority carrier lifetime of a FZ polished wafer (*n*-type, 5 Ω·cm) passivated with 10 nm thick a-Si:H layers: τ > 16 ms at 10^{15} cm^{-3}. Radiative and Auger recombination limits (according to Kerr *et al.* [3] and to Richter *et al.* [4]) are indicated by solid lines.

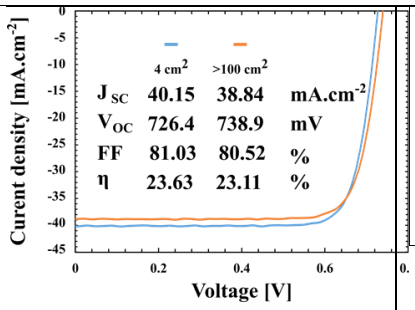

Fig. 2. Illuminated IV curves and cell parameters of the best both-sides-contacted SHJ solar cells (in-house measurements) on FZ *n*-type 230 µm thick 4" wafer 4cm^2 cell) and on CZ *n*-type 150 µm thick 6" wafer (for the >100cm^2 device).

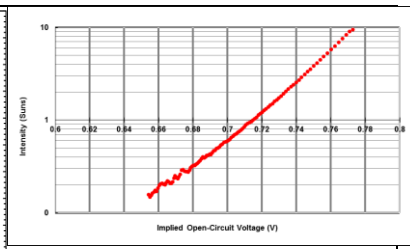

Fig 3. Implied Voc versus illumination curve for a 150 µm thick p-type Cz wafer symmetrically passivated with a firable hole-selective junction.