Area 3: III-V Compound Semiconductor and Concentrator and Space PV Technologies.

OPTIMIZATION OF SI BOTTOM SUBCELL FOR III-V ON SI WAFER BONDED MULTIJUNCTION SOLAR CELLS

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Multi-junction solar cells combining III–V top cells with a Si bottom cell offer the potential to increase the solar energy conversion efficiency beyond the 30% single-junction theoretical limit. In this work, monolithic 2-terminal triple junction (3J) GaInP/AlGaAs/Si solar cells of V_{OC} around 2.9V are produced by means of direct wafer bonding between GaAs and Si materials, which allows for a permanent, electrically conductive and optically transparent interface [1]. However, a large current mismatch between top III-V and bottom Si subcells severely limits the 3J performance (Fig. 1a). Varying Si subcell design and fabrication processes, we study the influence of the Si bottom subcell parameters on the 3J device performance.

GaInP/AlGaAs cells are grown in inverted configuration by MOVPE on 4" GaAs substrates at Fraunhofer ISE and then reported on n-on-p homo-junction Si cells by surface activated bonding. The Si solar cells are produced using 14-22 ohm.cm CZ or 1-5 ohm.cm FZ 4" (100) 525 µm-thick Si substrates. Using high minority carrier lifetime FZ Si substrates is expected to improve EQE at long wavelength in comparison to CZ substrates [2]. The formation of c-Si bottom cell with an optimum emitter, in terms of doping and thickness, at the front surface is critical to Si cell performance. Target doping profiles, which are dependent on III-V/Si interface recombination velocity [3], are defined using PC1D simulations. Doping is realized by diffusion or ion implantation processes (beam line or immersion plasma followed by thermal activation), allowing for doping profile tuning as shown in Fig. 1b. Back surface recombination is limited using an appropriate rear-side passivation [4]. In this study, the Si cells are produced on single-side polished substrates with Back Surface Field (BSF) and full sheet back metal contacts as well as on double-side polished substrates with BSF and PERC-like passivation using dielectric layers with point metal contacts. The III-V on Si layers are then processed into solar cells by: removal of GaAs substrate, mesa etching, deposition of front and back metal contacts, and a dual layer SiN_x/SiO_2 anti-reflective coating (ARC).

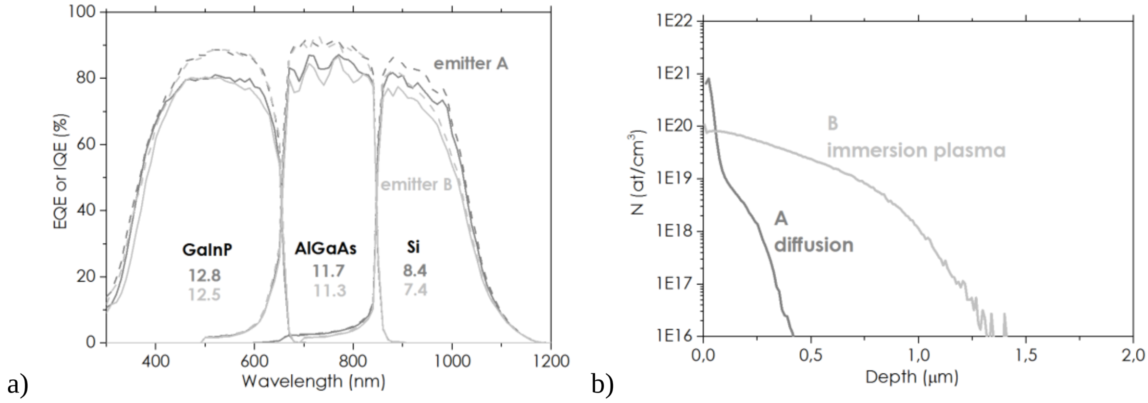

Figure 1: a) EQE (solid) and IQE (dashed lines) of n-on-p 3J III-V on Si. Subcell short-circuit current densities (J_{SC} in mA/cm²) are calculated from EQE under AM1.5G at 1000 W/m². b) Associated Si subcell emitter doping profiles as measured by SIMS.

EQE of resulting 3J devices with two different emitter doping profiles (Fig. 1a), reveals that the bottom Si sub-cell performance vary. Difference between top and middle subcells EQE are due to ARC thickness variations (IQE are similar). It should be pointed out that it is also possible to increase the current by optimizing the anti-reflective coating design. Ongoing Si subcell variations of a) Si substrates, b) emitter doping profiles and c) rear-side passivation are expected to bring large performance improvement.

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