Area 7: Performance and Reliability of PV Modules

INFLUENCE OF BIAS APPLICATION ON POTENTIAL INDUCED DEGRADATION FOR CRYSTALLINE SILICON PHOTOVOLTAIC MODULES

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Introduction: Recently, drastic decrease in output power of photovoltaic (PV) modules called potential-induced degradation (PID) has been reported as a degradation phenomenon in PV systems. PID may occur when a large potential difference is generated between the cell in the PV module and Al frame. It has been proposed that Na ions arising from the soda lime glass used as a front cover of the PV modules diffuse through the encapsulant into the cell surface and also inside of the cell and such Na ion diffusion is possible origin of PID for p-type crystalline Si PV modules [1]. As a consequence, the stacking faults are decorated by Na impurities. This results in significant shunting of the cells and degrades their efficiency [2]. Although significant progress has been made towards understanding the PID mechanisms, the influence of drifts of Na ions on the p-n junction has not been fully understood yet. In this study, we investigated the influence of bias directly applied to p-n junction during the PID test in order to clarify whether there is influence of change in band diagram or depletion layer width on Na drift. PID recovery test was also examined with or without bias application.

Experimental methods: Figure 1 shows the schematic diagram of the PID test. The PID test conditions are as follows: Forward bias or reverse bias was applied to p-n junction and the applied voltage was -1000 V between the back electrode of p-type cell and grounded Al plate on the front side of the glass. The module temperature was 85 °C, and the humidity was not controlled during the PID test (ca. 2% at 85°C). The PID recovery test was carried out with applied voltage of +1000 V between the cell and grounded Al plate on the front side of the glass. Other conditions were the same as the PID test.

Results and discussion: Figure 2 shows the normalized PV parameters after PID test. In the case that forward bias is applied to p-n junction during PID test, the higher bias voltage induces less PID with less degradation of fill factor. On the other hand, higher voltage of reverse bias application accelerates PID with drastic reduction in both open-circuit voltage and fill factor. The reason is considered as follows: Forward bias application to p-n junction during PID test may suppress drift of Na ions. On the other hand, reverse bias application to p-n junction during PID test may enhance the drift of Na ions. In PID recovery test, forward bias application suppresses recovery and reverse bias application accelerates recovery.

Conclusions: Influence of bias application to p-n junction during the PID test for p-type crystalline Si PV modules was studied. Higher forward bias voltage suppresses PID, on the other hand, higher reverse bias voltage accelerates PID. Such phenomena are possibly explained by suppression or enhancement of Na drift.

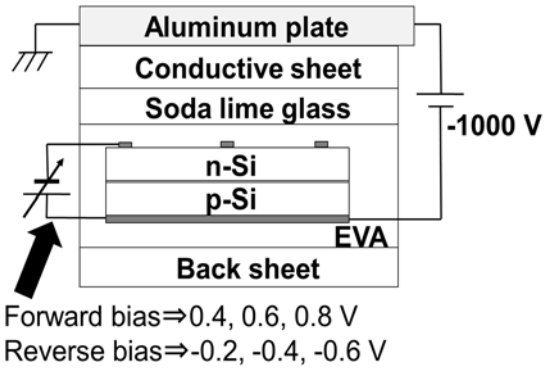

Figure 1: Schematic diagram of PID test.

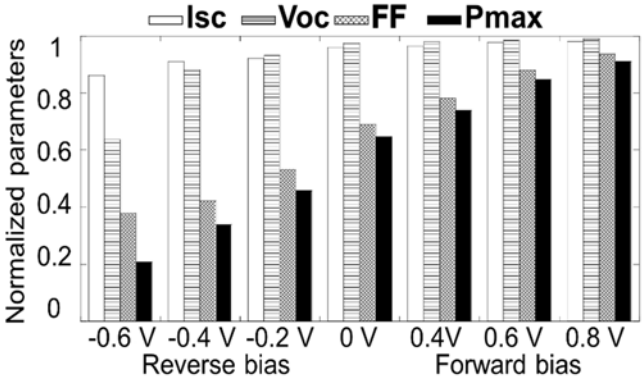

Figure 2: Normalized PV parameters after PID test.

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References:

[1] P. Hacke *et al.*: Proc. 37th IEEE PVSC, pp. 814-820 (2011).
[2] V. Naumann *et al.*: Sol. Energy Mater. Sol. Cells, **120**, 383-389 (2014).