Area: 1 Crystalline and Thin Film Silicon PV

REMOVING BARRIERS TOWARD THIN CRYSTALLINE SILICON SOLAR CELLS BY IMPROVED CRACK DETECTION USING DARK-FIELD IMAGING

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One of the challenges in today's photovoltaic (PV) industry is related to the high capital expenditure (capex) to manufacture crystalline silicon PV modules which comprises ~22% of the minimum sustainable price of PV modules [1]. In addition, nearly 58% of silicon capex is embedded in polysilicon and wafer manufacturing negatively affecting the cost-per-watt ($/W), levelized cost of electricity (LCOE, ¢/kWh) and prevents the scale up of the PV industry [1]. One path to lower capex is the reduction of the silicon usage per wafer by either reducing wafer thickness (see Fig. 1a) or growing silicon wafer via kerfless technologies. Si wafer thickness has decreased steadily over the years, but not as quickly as predicted despite the agreed cost benefits of thinner wafers. Handling and processing thin Si wafers (40 – 100 µm) is difficult and manufacturing yield is unacceptably low. Due to the brittle nature of silicon, wafer breakage is a major concern due to the high stress that is induced during process steps in manufacturing lines (*e.g.* sawing or the interconnection of cells). These high stresses induce edge cracks in wafers which can then further propagate creating a yield-based disincentive given today's low silicon prices. In particular, for a 180 µm thick wafer cracks smaller than 1 mm in length can lead to a breakage of 20% somewhere in the module production line [2]. Since thinner wafer will break with a smaller critical force, there is an industrial need for improvement in process steps and handling and even more important in crack detection tools. Current state-of-the-art industrially-available tools can only detect cracks which are longer than 1 mm in length with high enough sensitivity and repeatability.

Building on the industrially-available dark-field light scattering approach described in [2], we present an approach to image edge cracks with less than 500 µm in length. As seen in Fig. 1b, this is the required crack length to avoid high breakage rates (>50%) for wafers with a thickness of less than 100 µm. The goal of this work is to establish a reliable method for detecting edge micro-cracks by exploring the trade-off between field of view (FOV), incident light angle, and minimum detectable crack length. Secondly, the setup is further improved to unambiguously distinguish between an edge crack and a surface feature by decoupling the properties of light in the near infrared (NIR) and short wavelength infrared (SWIR) region due to the different absorption depths in silicon (see Fig. 1c and d). Thirdly, the scalability of this technique is explored including an analysis of minimum detectable crack length *vs.* wafer size for several cameras. Last, a techno-economic analysis is performed based on the calculated breakage rate to estimate the cost-of-tool ownership as a function of yield and wafer thickness.

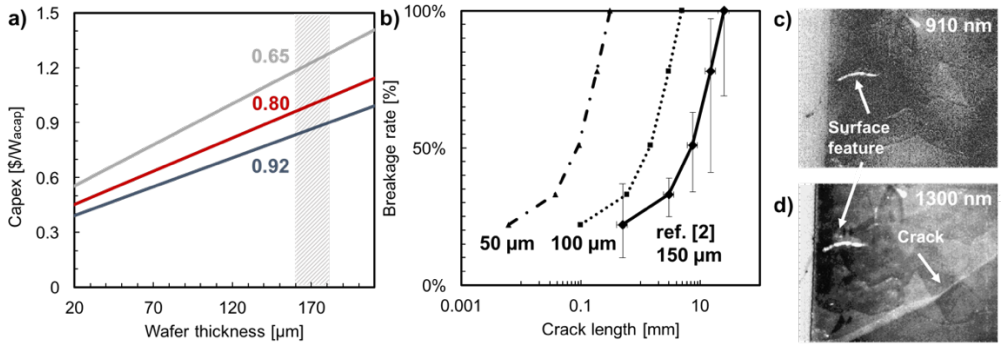

Figure 1: a) Total silicon PV capex as a function of wafer thickness, assuming constant yield from polysilicon to module. b) Crack length vs. breakage rate for different wafer thicknesses. c) and d) Scattering images taken at 910 and 1300 nm showing the decoupling of a surface features from a crack due to the different absorption depths in silicon.

References:
[1] D. Powell et al., Energy Env. Sci. 2015, 8, 3395–408.
[2] A. Ortner et al., Prog. Photovolt. Res. Appl. 2013, 21, 1343-53.